

## SECTION 7 MODULE SPECIFICATIONS

### 7.1 INTRODUCTION

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This section lists the specifications for the V.35/RS-449/X.21 Combined Data Interface Module. Listed separately are the specifications for the V.35, RS-449, and X.21 portions of this interface.

#### 7.1.1 V.35/306 Interface Specifications

The following are the specifications for the V.35 portion of this interface:

**Maximum Data Rate**

306 mode:	15 Mb/s
V.35 mode:	dependent upon cable length

**Clock and Data Tolerances**

Delay, SCT to SD:	70 ns typical
Skew, SCTE to SD:	20 ns typical

**Balanced Drivers**

Signal Swing (bipolar):	$\pm 0.55V \pm 0.1V$ into $100\Omega$
Short circuit current:	less than 100 mA
Rise time:	less than 20 ns
Generator impedance:	$100\Omega$

**Balanced Receivers**

Load resistance:	$100\Omega$
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**Polarity**

Data polarity:	Mark (binary 1): "A" lead negative with respect to "B" lead Space (binary 0): "A" lead positive with respect to "B" lead
Signaling polarity:	ON: greater than +3VDC OFF: open or less than -3VDC

#### 7.1.2 RS-449 Interface Specifications

The following are the specifications for the RS-449 portion of this interface:

**Maximum Speed**

RS-449 Balanced:	15 Mb/s synchronous timing
(RS-422 T - terminated)	20 kb/s asynchronous timing
(RS-422 U - unterminated)	520 kb/s recovered timing
RS-449 Unbalanced:	128 kb/s synchronous timing
(RS-423)	20 kb/s asynchronous timing
	128 kb/s recovered

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### Introduction

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#### **Polarity**

Data polarity: MARK (binary "1"): "A" lead negative with respect to signal ground  
SPACE (binary "0"): "A" lead positive with respect to signal ground

Signal polarity: OFF: "A" lead negative with respect to "B" lead  
ON: "A" lead positive with respect to "B" lead

#### **Unbalanced Drivers**

Short circuit current: 150 mA maximum  
Output Level (both states):  $0.9V_0$  (Open circuit voltage, into  $450\Omega$ )  
Output rise time (clock drivers): 1.2  $\mu$ s maximum  
Output rise time (signaling drivers): 10  $\mu$ s typical  
Open circuit voltage ( $V_0(>)$ ): 5.5  $\pm$  0.5 volts

#### **Balanced Drivers**

Short circuit current: 150 mA maximum  
Differential output signal swing: 2 volts minimum (with a  $100\Omega$  load)  
Output rise and fall time: 20 ns maximum  
Open circuit voltage: 6 volts maximum  
Average DC offset: 0V  $\pm$  0.4 volts

#### **Receivers**

Termination resistance: 100 $\Omega$ /unterminated  
(specified with fail safe networks) (RCV DATA, RCV CLK, EXT TX CLK)

Input impedance: 7.4 k $\Omega$  minimum  
6.6 k $\Omega$  minimum  
Single ended A to ground with B grounded

Input threshold:  $\pm$ 0.2 volts (A versus B)

### 7.1.3 X.21 Interface Specifications

The following are the specifications for the X.21 portion of this interface:

#### **Maximum Speed**

X.21: dependent upon cable length  
20 kb/s asynchronous timing  
520 kb/S recovered timing

#### **Polarity**

Data Polarity: MARK (binary "1"): "A" lead negative with respect to signal ground  
SPACE (binary "0"): "A" lead positive with respect to signal ground

Signal Polarity: OFF: "A" lead negative with respect to "B" lead  
ON: "A" lead positive with respect to "B" lead

**Drivers**

Short circuit current:	150 mA maximum
Differential output signal swing:	2 volts minimum (with a 100Ω load)
Output rise and fall time:	20 ns maximum
Open circuit voltage:	6 volts maximum
Average DC offset:	0V ±0.4 volts

**Receivers**

Termination resistance:	100Ω
(specified with fail safe networks):	(RCV DATA, RCV CLK, EXT TX CLK)
Input Impedance:	7.4 kΩ minimum 6.6 kΩ minimum Single ended A to ground with B grounded
Input threshold:	±0.2 volts (A versus B)

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**7.2 DIMENSIONS**

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The following are the dimensions for the V.35/RS-449/X.21 Combined Data Interface Module.

Width:	7.3 inches (185 mm)
Height:	1.5 inches (38 mm)
Depth:	5.2 inches (130 nun)

The Combined Data Interface Module fits into the interface slot for the FIREBERD 6000 and 4000 communications analyzers. Two spring-tensioned screws secure the interface module to the FIREBERD. Connector pins on the module mate with the mainframe's connector receptacle when the interface panel is flush with the mainframe rear panel.